Serial No: 10/726302
Examiner: J. Zweizig
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

REMARKS/ARGUMENTS

Reconsideration is requested in view of the following remarks.

Applicant has enclosed herein a partial translation of JP2001153924.

Claim Rejections – 35 USC §102

Claim 6 is rejected under 35 U.S.C. §102(b) as being anticipated by JP2001153924. Applicants respectfully traverse this rejection.

The semiconductor integrated circuit device according to claim 6 requires a plurality of power supply circuits connected to a common pad.

JP2001153924 discloses a reference voltage-generating circuit and a step-down circuit connected to a common pad. Although the step-down circuit is a power supply circuit, the reference voltage-generating circuit is not a power supply circuit. The reference voltage-generating circuit, more specifically, is a circuit for generating a voltage to be used in the step-down circuit and therefore cannot be reasonably interpreted by one skilled in the art as a power supply circuit. The semiconductor integrated circuit device disclosed in JP2001153924 therefore does not teach or suggest a plurality of power supply circuits connected to a common pad as required by claim 1 or claim 6 that depends from claim 1.

Further, claim 6 recites "the internal power supply generating circuits are capable of being all or selectively brought into a deactivated state." This feature advantageously allows the internal power supply generating circuit(s) to be deactivated before forcibly applying a power supply voltage externally, rather than internally via the internal power supply generating circuit(s), to the semiconductor integrated circuit device. The generation of an abnormal current or a through current caused by a collision between an output of the internal power supply generating circuit and the forcibly applied voltage from outside therefore can be prevented, allowing a desired voltage to be applied. JP2001153924 neither teaches nor suggests this feature of claim 6.

For at least these reasons, claim 6 as well as claims 7 and 8 that depend from claim 6, are patentable over JP2001153924. Claims 2-5 and 9 are allowed.

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Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

Respectfully submitted,

HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. Box 2902-0902
Minneapolis, MN 55402-0903
(612) 455-3800

Dated: 10/20/05

By: _____
Douglas P. Mueller
Reg. No. 30,300
DPM/dh

Partial Translation of JP 2001-153924

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Applicant: NIPPON ELECTRIC IC MICROCOMPUTER SYSTEM LTD

Inventor: Koichi GOTO

[0013]

[Mode for carrying out the invention] Next, the embodiments of the present invention are described below by reference to the drawings. Fig. 1 is a diagram in a schematic form depicting one example of layout of a chip in the semiconductor storage apparatus relative to first embodiment of the present invention. In comparison between Fig. 1 and Fig. 7, a chip 1A related to this embodiment is different from the chip 1C in conventional semiconductor storage apparatus, in that:

(1) the number of pad for voltage measurement is decreased to one (pad 2), and the output voltage of a reference voltage-generating circuit 12 and the output voltage of a step-down circuit 13 are output via the one and same pad 2;

(2) a p-channel MOS transistor (pMOS transistor) P1 is inserted between the output point of the reference voltage-generating circuit 12 and the pad 2, and a pMOS transistor P2 is inserted between the output point of the step-down circuit 13 and the pad 2, in such a manner as to form their respective current paths; and

(3) a test circuit 14 is added to a test circuit block 11A in order to control the

on/off states of the above mentioned pMOS transistors P1 and P2.

[0014] A signal C1 from the test circuit 14 is input to the gate electrode of the pMOS transistor P1, while a signal C2 from the same test circuit 14 is input to the gate electrode of the pMOS transistor P2. The two signals C1 and C2 are complementary signal to each other. When the storage apparatus has entered into the test mode according to a chip select signal CS, a row address strobe signal RAS, a column address strobe signal CAS and a write enable signal WE, the test circuit 14 is activated by a signal resulting from decoding of an address signal A_n. The output signals C1 and C2 exchange levels depending on whether the test circuit 14 is in an inactive state or an active state, while maintaining a complementary relationship between the two.

[0015] Fig. 2 shows the operating waveforms of the signals in this embodiment. Referring to Fig. 2, when the chip select signal CS, the row address strobe signal RAS, the column address strobe signal CAS and the write enable signal WE input from outside to the chip 1A change from high level to low level at a time T10, the storage apparatus enters into the test mode at the rising edge of a clock signal CLK immediately after that (time T11), thereby activating the test circuit 14. Prior to the time T11, the storage apparatus is in the normal storage operation mode and the test circuit is in a deactivated state.

[0016] Now, if the storage apparatus is in the normal storage operation mode prior to the time T11, the test circuit 14 is in the inactive state and outputs the high-level signal C1 and the low-level signal C2. Accordingly, the pMOS transistor P1 is off state and the pMOS transistor P2

is on state, and an internal power voltage V_{INT} from the step-down circuit 13 is output to the pad 2.

[0017] When the storage apparatus enters into the test mode at the time T11, concurrently with that, the output signal C1 of the test circuit 14 changes from high level to low level and the signal C2 of the test circuit 14 changes from low level to high level. This allows the pMOS transistor P1 to switch from off state to on state and the pMOS transistor P2 to switch from on state to off state, and then a reference voltage V_{REF} from the reference voltage-generating circuit 12 is output to the pad 2.

[0018] According to this embodiment, by activating the test circuit 14 through entry into the test mode, it is possible to measure the output voltage directly by means of one pad by switching between the output voltage of the reference voltage-generating circuit and the output voltage of the step-down circuit. In that case, since the chip select signal CS, the row address strobe signal RAS, the column address strobe signal CAS, the write enable signal WE and even the address signal An are all necessary for normal storage operation, there is no need for an additional control signal for switching between the output voltages to the pad 2 or an additional pad for input of the control signal. Consequently, the number of pad is decreased by one in the entire storage apparatus.

[0019] In the case of this embodiment, the following components are to be added: (1) two pMOS transistors (P1 and P2); (2) test circuit 14; and (3) wiring between the test circuit 14 and the gate electrodes of the pMOS transistors P1 and P2. Also, (4) it is necessary to add a structure for selecting and activating/deactivating the test circuit 14, to the decoder for

the address signal An. Still, since the area required for that addition is smaller by far than the area of one pad, it is possible to downsize the area of the entire chip by an area approximately equivalent to one pad. In a typical high-capacity DRAM of 128 Mbits, for example, the pad is generally a square of about 100 μm x 100 μm per one. On the contrary, the MOS transistors used in a high-capacity DRAM of 128Mbits, forming an internal circuit inside the chip, are typically about 1.0 μm and 0.7 μm in channel length. In addition, as described later, the test circuit 14 constitutes about eight MOS transistors at the most, and also it is estimated that the addition of the structure to the decoder for the address signal An requires only several transistors. Therefore, the area increased for the reasons relative to the above mentioned test circuit 14 and the aforesaid additional components (1) to (4) accounts for as little as several percent of one pad. Moreover, whereas an increase in number of pads would affect the chip area because the pads need to be regularly arranged on the edge of the chip, the transistors of the test circuit, the MOS transistors P1 and P2 as switches and the wiring can be laid out at some empty space in the chip. Consequently, in an extreme case, it could be said that this addition has no effect on the area of the chip.

[0020] In this embodiment, the p-channel MOS transistors are inserted between the output point of the reference voltage-generating circuit 12 and the pad 2, and between the output point of the step-down circuit 13 and the pad 2. Alternatively, these transistors may be composed of n-channel MOS transistors. In this case, however, there occur potential differences between the pad 2 and the output point of the reference voltage-generating circuit 12, and between the pad 2 and the output point of

the step-down circuit 13, due to so-called "falling below the threshold" in the nMOS transistors (a phenomenon in which, when a drain voltage and gate voltage are provided to an nMOS transistor, a source voltage does not exceed a value obtained by subtracting the threshold voltage of the transistor from the gate voltage). Thus, in order to accurately measure the reference voltage V_{REF} and the step-down power voltage V_{INT}, it is required to make a correction to the measured voltage value of the pad 2, based on the threshold voltage of the nMOS transistor.

[0021] Next, the second embodiment of the present invention is described below. Fig. 3 is a schematic diagram showing one example of layout of a chip in the semiconductor storage apparatus related to the second embodiment of the present invention. In comparison of Fig. 3 and Fig. 1, the chip 1B of this embodiment is different from the chip 1A of the first embodiment, in that:

(1) nMOS transistors N1 and N2 are used instead of the pMOS transistors;

(2) a step-up output voltage V_B from the step-up circuit 15 is input to the gate electrodes of the nMOS transistors N1 and N2, via the pMOS transistors P3 and P4, respectively; and

(3) the pMOS transistors P3 and P4 are turned on or off in a complementary manner by the signals C1 and C2 from the test circuit 14.

[0022] The step-up circuit 15 is a circuit that raises an external power voltage Vcc to a higher voltage $Vcc + \alpha$ ($= V_B$). In a high-capacity DRAM, for example, the step-up circuit 15 applies a high voltage to a word line in order to prevent a drop in signal voltage read from a memory cell composed of one transistor and one capacitor to a data line or written from

the data line to the memory cell, due to falling below the threshold in the nMOS transistor as a switch. Conventionally, this circuit is essential to high-capacity semiconductor storage apparatuses. This embodiment also uses a circuit from such a conventional semiconductor storage apparatus, and thus there is no need to newly provide the step-up circuit 15, causing no are increase of the chip.

[0023] Fig. 4 shows the operating waveforms of signals in this embodiment. Referring to Fig. 4, in this embodiment as well as in the first embodiment, the storage apparatus enters into the test mode from the normal storage operation mode at the rising edge of a clock signal CLK (time T21) immediately after the row address strobe signal RAS, the column address strobe signal CAS, and the write enable signal WE fell from high level to low level at the time T20.

[0024] Now, if the storage apparatus is in the normal storage operation mode prior to the time T21, the test circuit 14 is in the inactive state and outputs the high level signal C1 and the low level signal C2. Therefore, out of the two pMOS transistors connected to the output point of the test circuit 14, the transistor P3 is off state. On the other hand, the pMOS transistor P4 is on state and transfers the output voltage V_B of the step-up circuit 15 to the gate electrode of the nMOS transistor N2 connected to the pad 2. As the result, out of the two nMOS transistors connected to the pad 2, the transistor N1 is off state, and the nMOS transistor N2 is on state and outputs to the pad 2 the internal power voltage V_{INT} from the step-down circuit 13. At this time, the output voltage V_B of the step-up circuit 15 applied to the gate electrode of the nMOS transistor N2 is raised to

a higher voltage Vcc+ α than the power voltage Vcc, and thus there is no falling below the threshold in the nMOS transistor N2. Accordingly, the internal power voltage V_{INT} is output as it is to the pad 2, and it is not necessary to make a correction to the measured value of the internal power voltage V_{INT}.

[0025] Next, when the storage apparatus enters into the test mode at the time T21, the output signal C1 of the test circuit 14 changes from high level to low level and the signal C2 changes from low level to high level. Hereby, out of the two pMOS transistors connected to the test circuit 14, the transistor P3 switches from off state to on state, and the pMOS transistor P4 switches to off state. As a consequence, out of the two nMOS transistors connected to the pad 2, the transistor N1 is provided with the output voltage V_B of the step-up circuit to the gate electrode and changes from off state to on state. On the other hand, the nMOS transistor N2 changes from on state to off state, and outputs to the pad 2 the reference voltage V_{REF} from the reference voltage-generating circuit 12. At this time, the output voltage V_B of the step-up circuit 15 applied to the gate electrode of the nMOS transistor N1 is raised to a higher voltage Vcc + α than the power voltage Vcc, and thus there is no falling below the threshold in the nMOS transistor N1. Therefore, the reference power voltage V_{REF} is output as it is to the pad 2, and it is not necessary to make a correction to the measured value of the reference power voltage V_{REF}.

[0026] Fig. 5 is a circuit diagram showing one example of the test circuit 14 in this embodiment. The test circuit 14 depicted in this figure is activated when the decode output of the address signal A_n is high level, and

is in an inactive state when the decode output is low level. Now, if the decode output is low level and the test circuit 14 is in an inactive state, that is, prior to the time T21 in the timing chart shown in Fig. 4, the nMOS transistor N5 is on state, the nMOS transistor N7 is off state, and the pMOS transistor P4 is on state. In addition, the nMOS transistor N6 is off state, the nMOS transistor N8 is on state, and the pMOS transistor P3 is off state. Accordingly, in Fig. 3, the nMOS transistor N2 is provided with the step-up voltage $V_B = Vcc + \alpha$ to the gate electrode through the pMOS transistor P4 and is thus brought into conduction, and outputs to the pad 2 the output voltage V_{INT} of the step-down circuit. On the other hand, the nMOS transistor N1 shuts down a connection between the output point of the reference voltage-generating circuit 12 and the pad 2.

[0027] On the other hand, if the decode output is low level and the test circuit 14 is in an inactive state, that is, after the time T21 in the timing chart shown in Fig. 4, the nMOS transistor N5 is off state, the nMOS transistor N7 is on state, and the pMOS transistor P4 is off state. In addition, the nMOS transistor P6 is on state, the nMOS transistor N8 is off state, and the pMOS transistor P3 is on state. Accordingly, in Fig. 3, the nMOS transistor N1 is provided with the step-up voltage V_B to the gate electrode through the pMOS transistor P3 and is thus brought into conduction, and outputs to the pad 2 the output voltage V_{REF} of the reference voltage-generating circuit. On the other hand, the nMOS transistor N2 shuts down a connection between the output point of the step-down circuit 13 and the pad 2.

[0028] As a matter of course, the test circuit 14 shown as one example

in Fig. 5 is also applicable to the storage apparatus related to the first embodiment. In the second embodiment, however, the step-up voltage V_B is turned on or off unlike in the case of the first embodiment, and thus it is desired to, for the nMOS transistors N5 and N6 in the test circuit 14, use the transistors of larger sizes than those in the first embodiment, about 3.0μm in gate width and 1.0μm in gate length, considering that a highly strong electric field is applied to these transistors. Also, as distinct from the first embodiment, this embodiment requires the two additional pMOS transistors P3 and P4. Accordingly, the area of them is increased by just that much than the area in the first embodiment, but the increase is negligible in comparison the area of one pad.

[0029]

[Effect of the Invention] According to the present invention, it is possible to monitor and measure the output voltage of the reference voltage-generating circuit and the output voltage of the step-down circuit by means of the one and same pad, which would require two pads conventionally. Consequently, the area of the chip can be decreased by the omitted pad.

[0030] Applicable to the analog switch is pMOS transistor or nMOS transistor. In using an nMOS transistor as an analog switch, it is necessary to make a correction to the measured value based on the falling-below-threshold phenomenon in the nMOS transistor. In that case, the correction of the measured value becomes unnecessary by configuring the storage apparatus in such a manner that the output voltage of the step-up circuit generally contained in the conventional storage apparatus is input to

the gate electrode of the nMOS transistor as an analog switch.

[Fig. 1]

(1) Chip

(2) Test circuit block

(3) Test circuit

(4) Pad

(5) Reference voltage-generating circuit

(6) Step-down circuit

[Fig. 2]

(1) Address signal

(2) Output voltage to pad 2

[Fig. 3]

(1) Chip

(2) Step-up circuit

(3) Test circuit

(4) Reference voltage-generating circuit

(5) Step-down circuit

(6) Test circuit block

[Fig. 4]

(1) Address signal

(2) Output voltage of pad 2

[Fig. 5]

(1) Test circuit

(2) Step-up voltage

(3) Step-up voltage

(4) Address signal decode output

(5) "H" at enable time

"L" at disable time

(6) Step-up voltage

(7) Step-up voltage

(8) To nMOS transistor N_2

(9) To nMOS transistor N_1

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【図６】半導体記憶装置における、外部電源電圧と、内部電源電圧と、基準電圧との関係の一例を示す図である。

【図７】従来の技術による半導体記憶装置におけるチップのレイアウトの一例を模式的に示す図である。

【符号の説明】

１Ａ，１Ｂ，１Ｃ　チップ　＊

12

＊２　パッド

１１Ａ，１１Ｂ　テスト回路ブロック

１２　基準電圧発生回路

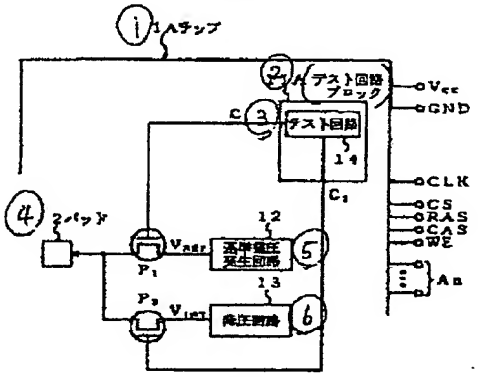
１３　降圧回路

１４　テスト回路

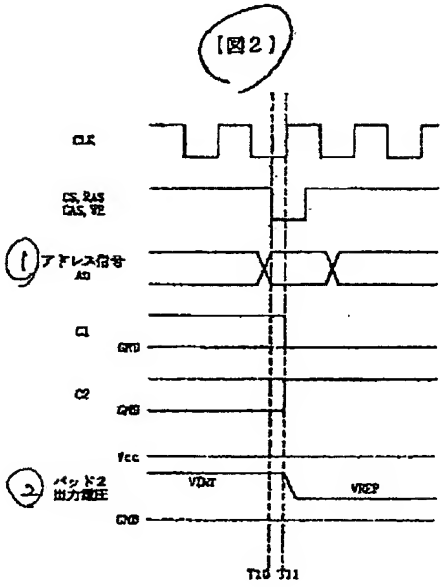
１５　昇圧回路

２０，２１　パッド

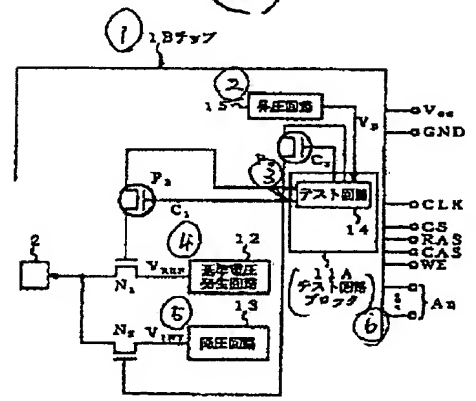
【図１】



【図２】



【図３】



【図４】